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This is a communication from the examiner in charge of your application.
COMMISSIONER OF PATENTS AND TRADEMARKS

☑ This application has been examined ☐ Responsive to communication filed on _____ ☐ This action is made fina

A shortened statutory period for response to this action is set to expire 3 month(s), 0 days from the date of this letter. Failure to respond within the period for response will cause the application to become abandoned. 35 U.S.C. 133

Part I THE FOLLOWING ATTACHMENT(S) ARE PART OF THIS ACTION:

1. ☑ Notice of References Cited by Examiner, PTO-892.
2. ☑ Notice of Draftsman's Patent Drawing Review, PTO-948
3. ☑ Notice of Art Cited by Applicant, PTO-1449.
4. ☐ Notice of Informal Patent Application, PTO-152.
5. ☐ Information on How to Effect Drawing Changes, PTO-1474..
6. ☐ _____

Part II SUMMARY OF ACTION

1. ☑ Claims 1-20 are pending in the application
   Of the above, claims _____ are withdrawn from consideration.
2. ☐ Claims _____ have been cancelled.
3. ☐ Claims _____ are allowed.
4. ☑ Claims 1-20 are rejected.
5. ☐ Claims _____ are objected to.
6. ☐ Claims _____ are subject to restriction or election requirement.
7. ☐ This application has been filed with informal drawings under 37 C.F.R. 1.85 which are acceptable for examination purposes.
8. ☐ Formal drawings are required in response to this Office action.
9. ☐ The corrected or substitute drawings have been received on _____. Under 37 C.F.R. 1.84 these drawings are ☐ acceptable; ☐ not acceptable (see explanation or Notice of Draftsman's Patent Drawing Review, PTO-948).
10. ☐ The proposed additional or substitute sheet(s) of drawings, filed on _____. has (have) been ☐ approved by the examiner; ☐ disapproved by the examiner (see explanation).
11. ☐ The proposed drawing correction, filed _____, has been ☐ approved; ☐ disapproved (see explanation).
12. ☐ Acknowledgement is made of the claim for priority under 35 U.S.C. 119. The certified copy has ☐ been received ☐ not been received ☐ been filed in parent application, serial no. _____; filed on _____.
13. ☐ Since this application apppears to be in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under Ex parte Quayle, 1935 C.D. 11; 453 O.G. 213.
14. ☐ Other

EXAMINER'S ACTION

Part III DETAILED ACTION

Drawings

1. The drawings are objected to because Fig.3 does not show power supply rail 124 as recited in lines 3 and 19, page 13, lines 11 and 27, page 14 of the specification; all elemments in amplifier stage 114 in Fig.3 should have numerical labels such as elements 116, 118 and 126. Correction is required.

2. The drawings are objected to under 37 C.F.R. § 1.83(a). The drawings must show every feature of the invention specified in the claims. Therefore, the sourcing circuitry having an NPN bipolar junction transistor being coupled to an emitter of the PNP transistor to form a Darlington pair as recited in claims 3 and 14 must be shown or the feature cancelled from the claim. No new matter should be entered.

Specification

3. The disclosure is objected to because of the following informalities: all elements in amplifier stage 114 in Fig.3 should be described or defined such as elements 116, 118 and 126. Appropriate correction is required.

Claim Rejections - 35 USC § 112

4. Claims 1-2, 4-13 and 15-20 are rejected under 35 U.S.C. § 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

In claim 1, there is no antecedent basis for "said mirroring circuitry" (lines 13-14, 20-21 and 23).

In claim 4, there is no antecedent basis for "said mirroring circuitry" (lines 8-9).

In claim 6, there is no antecedent basis for "said mirroring circuitry" (lines 1-2). It is not clear how the resistor being coupled between an emitter of the NPN bipolar junction transistor and a ground potential can control the rate of increase of current through the mirroring circuitry as the output stage performs the sinking operation. A resistor can not control any rate of increase of any current.

In claim 7, there is no antecedent basis for "said mirroring circuitry" (lines 1-2). It is not clear how the predetermined lower voltage limit established by the voltage clamp can prevent the NPN bipolar junction transistor from interfering with the sinking circuitry during the sinking operation since the NPN bipolar junction transistor must control the sinking circuitry during the sinking operation and must be interfering with the sinking circuitry.

Claim 8 is similarly rejected as claim 7.

In claim 11, there is no antecedent basis for "said mirroring circuitry" (lines 1-2).

In claim 12, the generation of the "current" (line 11) is not clearly defined. It is not clear how the mirroring transistor can draw current from the current balancing circuit since the current balancing circuit is defined as being controlled by the mirroring transistor (lines 13-15). Therefore, the current balancing circuit must draw current from the mirroring transistor to control the sourcing transistor.

In claim 17, it is not clear how the predetermined lower voltage limit established by the voltage clamp can prevent the NPN bipolar junction transistor from interfering with the sinking circuitry during the sinking operation (lines 4-7) since the NPN bipolar junction transistor must control the sinking circuitry during the sinking operation and must be interfering with the sinking circuitry. It is not clear how the resistor coupled between an emitter of the NPN bipolar junction transistor and a ground potential can control the rate of increase of current through the mirroring circuitry as the output stage performs the sinking operation (lines 8-11). A resistor can not control any rate of increase of any current.

In claim 19, the generation of "the current" (line 9) is not defined.

Claims 2, 5, 9-10, 13, 15-16 and 20 are rejected as being vague and indefinite for being dependent on the above respective rejected claims 1, 4, 6-8, 11-12, 17 and 19.

Claim Rejections - 35 USC § 102

5. The following is a quotation of the appropriate paragraphs of 35 U.S.C. § 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless --
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

6. Claims 1, 6, 11-12 and 19 are rejected under 35 U.S.C. § 102(b) as being anticipated by the Article of "Motorola Linear/Interface Devices", cited by Applicant.

The top circuit on page 2-258 of the Article of "Motorola Linear/Interface Devices", cited by Applicant, reads on claim 1 as follows

input amplifier stage of transistors Q5-Q6 and Q11-Q12; sourcing transistors Q17-Q18 for sourcing an output current to an external output load; sinking transistor Q16 being coupled to sourcing transistor Q17-Q18 for sinking a current from the external output load wherein sourcing transistors Q17-Q18 and sinking transistor Q16 having a common output node; transistors Q13-Q14 responsive to input amplifier stage of transistors Q5-Q6 and Q11-Q12 and

being coupled to sinking transistor Q16; current mirroring transistors Q8 and Q15 responsive to transistors Q13-Q14 to control sourcing transistors Q17-Q18; in response to a first predetermined output from input amplifier stage of transistors Q5-Q6 and Q11-Q12, transistors Q13-Q14 being switched ON to pull down almost the current from the collector of current mirroring transistor Q15 causing an insignificant current to flow in sourcing transistors Q17-Q18 and causing sinking transistor Q16 to sink a significant current from the external output load; in response to a second predetermined output from input amplifier stage of transistors Q5-Q6 and Q11-Q12, transistors Q13-Q14 being switched OFF blocking almost the current from the collector of current mirroring transistor Q15 to cause a significant current flowing in sourcing transistors Q17-Q18.

Claim 6 is similarly rejected as claim 1 and further: resistor R15 being connected between the emitter of NPN transistor Q13 and ground.

Claim 11 is similarly rejected as claim 1 and further: transistors Q13-Q14 being NPN bipolar junction transistors being coupled to form a Darlington pair.

Claim 12 is similarly rejected as claim 1.

Claim 19 is similarly rejected as claims 1, 6 and 11-12 for reciting the method of the apparatus as recited in claims 1, 6 and 11-12.

Claim Rejections - 35 USC § 103

7. The following is a quotation of 35 U.S.C. § 103 which forms the basis for all obviousness rejections set forth in this Office action:

> A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.
>
> Subject matter developed by another person, which qualifies as prior art only under subsection (f) or (g) of section 102 of this title, shall not preclude patentability under this section where the subject matter and the claimed invention were, at the time the invention was made, owned by the same person or subject to an obligation of assignment to the same person.

8. Claims 2 and 13 are rejected under 35 U.S.C. § 103 as being unpatentable over the Article of "Motorola Linear/Interface Devices", cited by Applicant.

What is not shown in the top circuit on page 2-258 of the Article of "Motorola Linear/Interface Devices", cited by Applicant, is the sourcing circuitry comprising a PNP bipolar junction transistor as recited in claim 2.

The sourcing circuitry comprising a PNP bipolar junction transistor as recited in claim 2 is operable for sourcing an output current to an external output load.

Sourcing NPN bipolar junction transistors Q17-Q18 in

the top circuit on page 2-258 of the Article of "Motorola Linear/Interface Devices", cited by Applicant, are also operable for sourcing an output current to an external output load.

Absence any showing of criticality for the specific operation of the claimed sourcing circuitry comprising a PNP bipolar junction transistor, sourcing NPN bipolar junction transistors Q17-Q18 in the top circuit on page 2-258 of the Article of "Motorola Linear/Interface Devices", cited by Applicant, is seen to provide the same desired function of sourcing an output current to an external output load such as that of the claimed sourcing circuitry comprising an PNP bipolar junction transistor as recited claim 2. It is merely a matter of design choice for the conductivity type of transistor. Therefore, the claimed sourcing circuitry comprising a PNP bipolar junction transistor as recited in claim 2 is rendered obvious by sourcing NPN bipolar junction transistors Q17-Q18 in the top circuit on page 2-258 of the Article of "Motorola Linear/Interface Devices", cited by Applicant.

Claim 13 is similarly rejected as claim 13.

Double Patenting

9. Claims 1, 6-12 and 17-20 provisionally rejected under the judicially created doctrine of obviousness-type double patenting

as being unpatentable over claims 1, 5-10, 12, 14-15 and 19-20 of copending application Serial No. 08/348,662. Although the conflicting claims are not identical, they are not patentably distinct from each other because the current source as recited in lines 15-16 of claim 1 and lines 14-15 of claim 12 of the copending application Serial No. 08/348,662 is obviously responsive to the current mirroring circuitry and is obviously coupled to provide current signal for controlling the sourcing circuitry such as the current balancing circuit as recited in lines 14-16 of claim 1 and lines 13-15 of claim 12 of the present application.

This is a *provisional* obviousness-type double patenting rejection because the conflicting claims have not in fact been patented.

10. The obviousness-type double patenting rejection is a judicially established doctrine based upon public policy and is primarily intended to prevent prolongation of the patent term by prohibiting claims in a second patent not patentably distinct from claims in a first patent. *In re Vogel*, 164 USPQ 619 (CCPA 1970). A timely filed terminal disclaimer in compliance with 37 C.F.R. § 1.321(b) would overcome an actual or provisional rejection on this ground provided the conflicting application or patent is shown to be commonly owned with this application. See 37 C.F.R. § 1.78(d).

Allowable Subject Matter

11. Claims 4-5 and 15-16 would be allowable if rewritten to overcome the rejection under 35 U.S.C. § 112 and to include all of the limitations of the base claim and any intervening claims.

Conclusion

12. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

See Matsumura, Yoshida and Stockstad et al, generally, for the current amplifier circuit. Relevant to claims 1, 12 and 19.

13. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Examiner Trong Phan whose telephone number is (703) 308-4870.

TP

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March 31, 1995

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